DESIGNING THE FUTURE ™

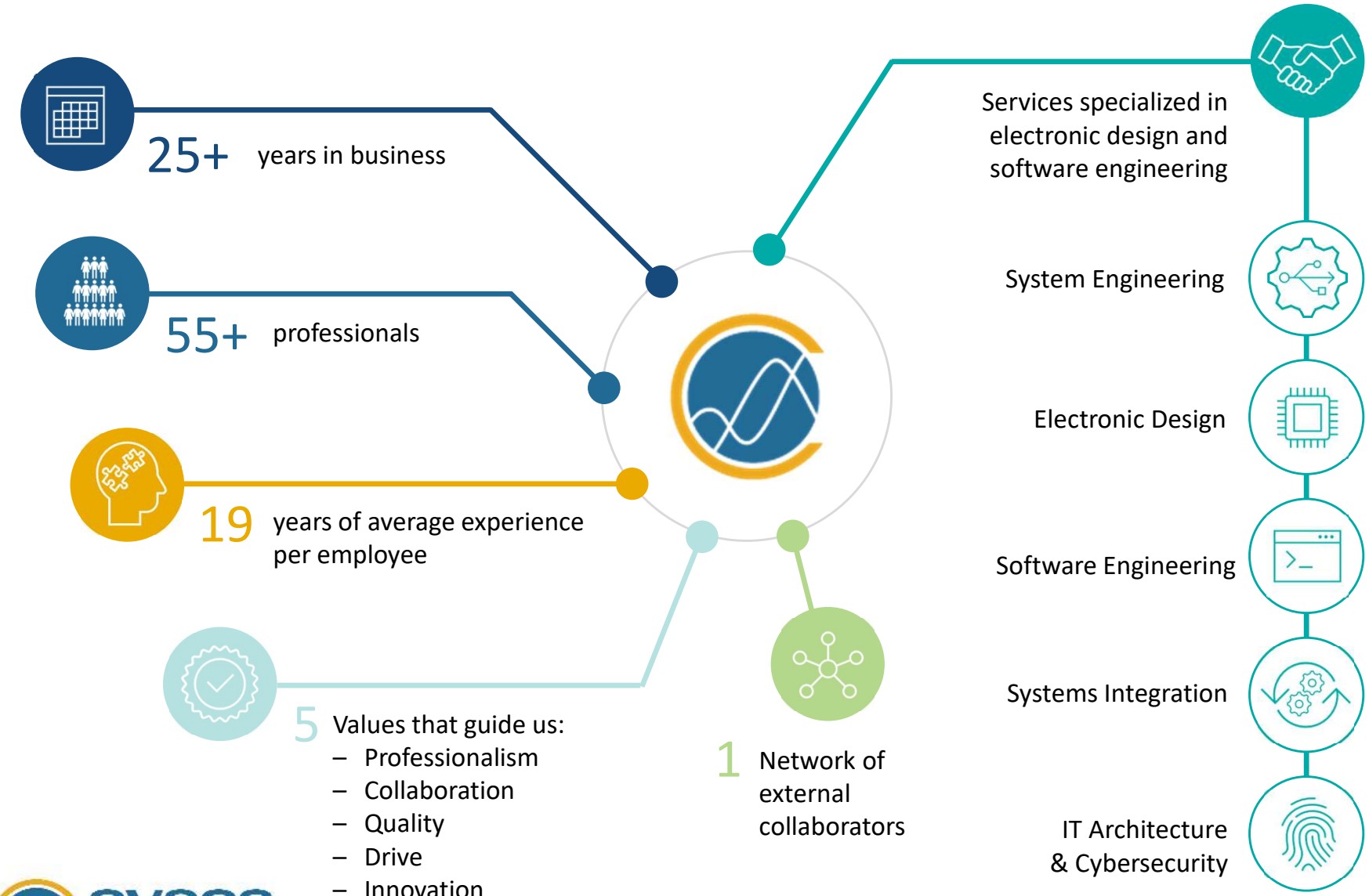
Cysca Technologies

# Design and Simulation of a SiC Totem-Pole PFC for EV Onboard Charging

June 17, 2026

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# A Glimpse into Cysca




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# Cysca Mission

**Our purpose**

**Our mission is to support our clients' ambitions** through leveraging our expertise in developing electronic systems, the related embedded software and user interface applications, while bringing forth our creativity and innovative mindset.



**Creating innovative solutions for technological headway**

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# Cysca Vision

**Our vision is to be recognized as the reference for efficient technological solutions**, including in areas where **safety and security are critical**. We aim to harness innovation for the benefit of sustainable growth.



**Being a premier engineering firm committed to technological innovation and the creation of value through sustainable growth**

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# Cysca Team

| Engineers | Professionals | Technicians |
| --- | --- | --- |
| • Software Engineers<br>• Electrical Engineers<br>• Mechanical Engineers | • Software Specialists<br>• Embedded and Firmware Specialists<br>• Electronic Specialists<br>• Test Specialists<br>• QA and documentation | • Electrical Technicians<br>• Drafting, CAD and PCB Layouts<br>• Manufacturing and Assembly Technicians<br>• Electrician and Field Support Technicians |

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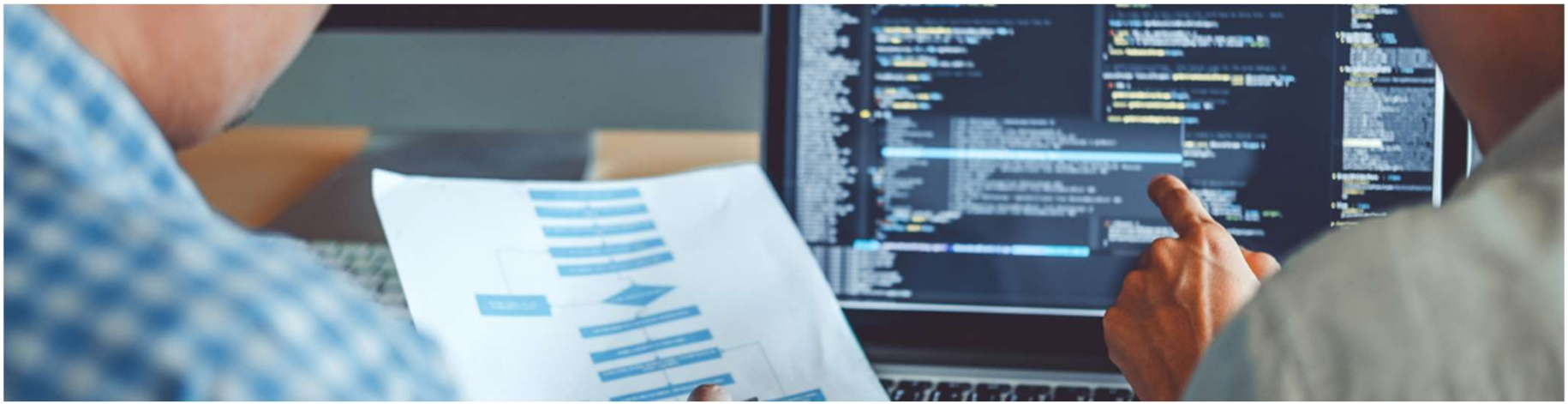
# Systems Engineering

- Turnkey projects
- Technical analysis
- Architecture Development
- Project management
- Public tender preparation
- Technical documentation
- Obsolescence management
- FMEA
- ….



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# Software Engineering



- Requirements
- Architecture, Coding
- Testing, Validation
- Embedded software development
- Expertise in IEEE software development process and multiple other standards
- OS less and RTOS based systems
- Distributed applications, on Windows or Linux
- Web applications
- Databases and servers
- Integration with various advanced systems, including ERP, DevOps, SCADA, AI...
- Support and modernization of existing applications

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# System / Software Engineering Case

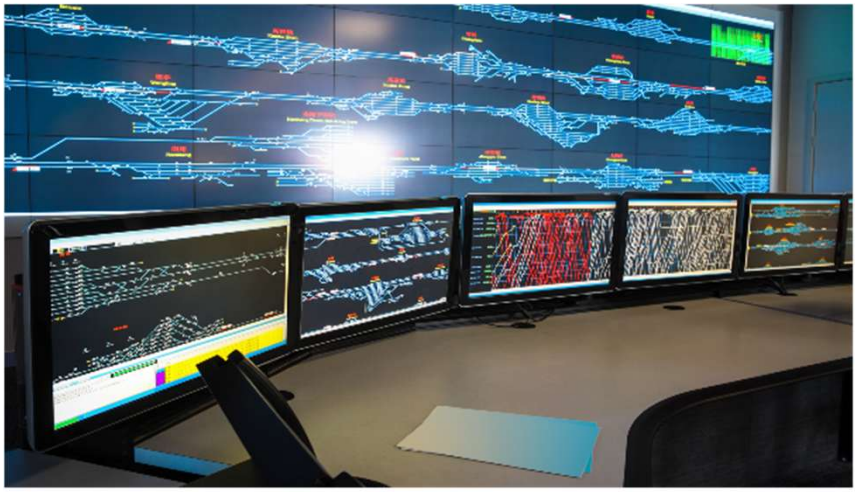


- Cysca has developed a proximity detector for the railway industry.
- The detector is used to provide driving assistance and warn locomotive drivers of the presence of vehicles on the track.
- As part of this project, Cysca also developed a test bench to validate all software functionalities and the detector's interfaces. This tool assists the client with maintenance, diagnostics, and troubleshooting.
- Cysca also improved and upgraded a more powerful server to perform remote software updates and ensure real-time monitoring of the client's entire fleet.

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# Systems Integration



- Integration of complex systems
- Information Technology for trains and busses (ITS)
- Internet of Things (IoT) Solutions
- Certification activities Management
- Industrial controls
- Building controls / Automation
- System Validation / Test Bench Development

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# Systems Integration Case

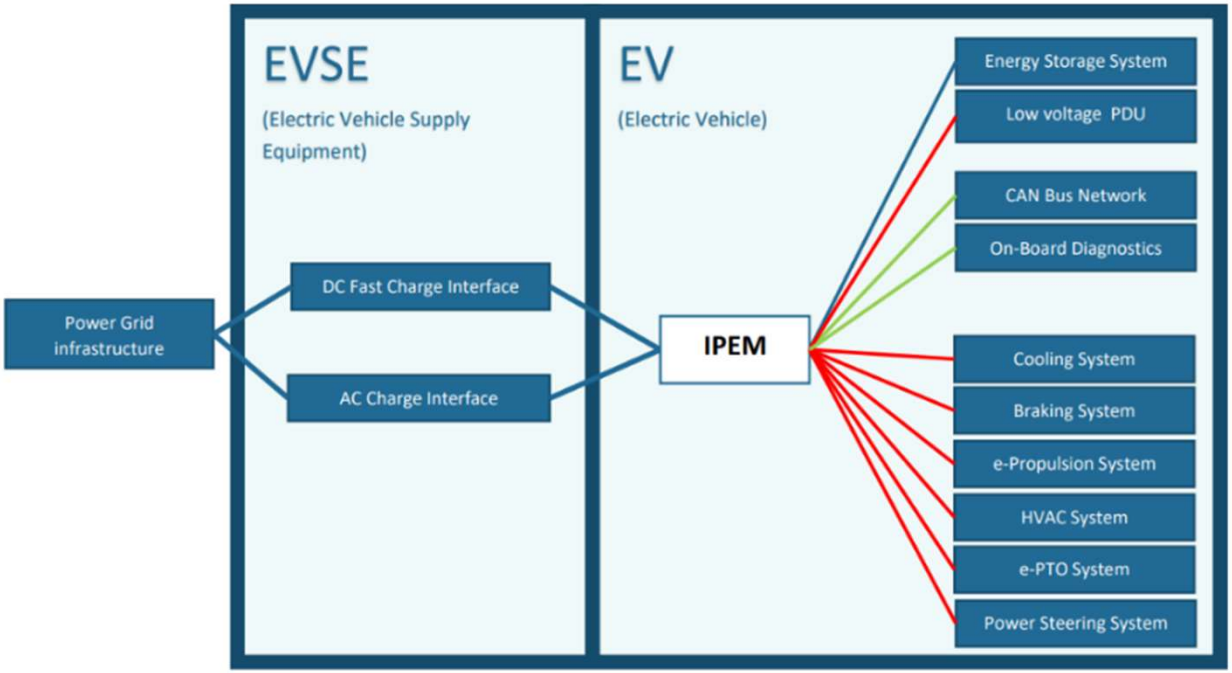



*Figure 1 – IPEM Context diagram*

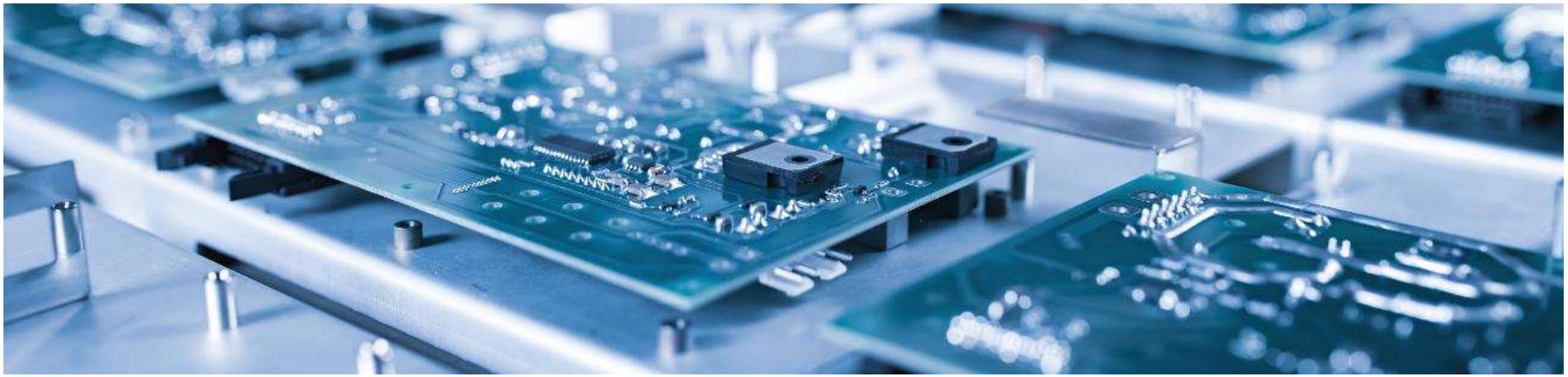
For the automotive industry, North American Class 3 to Class 8 vehicles. Cysca has developed a 3-in-1 IPEM (Integrated Power Electronic Module) by integrating off-the-shelf battery chargers, DC/DC converters, charge control unit and by designing custom junction box and embedded software.

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# Electronic Design



- Leader in design and development of custom electronic circuits over more than two decades
- Controllers for mass transit, railway, defense, industrial, aerospace,…
- User-Machine Interfaces (UMI)



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# Electronic Design Cases




**For the emergency vehicles**, Cysca has developed a complete secure connected hub use to manage and control sirens, lights, IT applications, radios, everything…



**For the food industry**, Cysca has developed the control system of a high-speed combination scale using distributed processing architecture and high-performance real-time system.



**For the power and energy metering industry**, Cysca has developed a variety of transducers interfacing current sensor such as Rogowski coil and voltage sensor.

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# IT Architecture & Cybersecurity





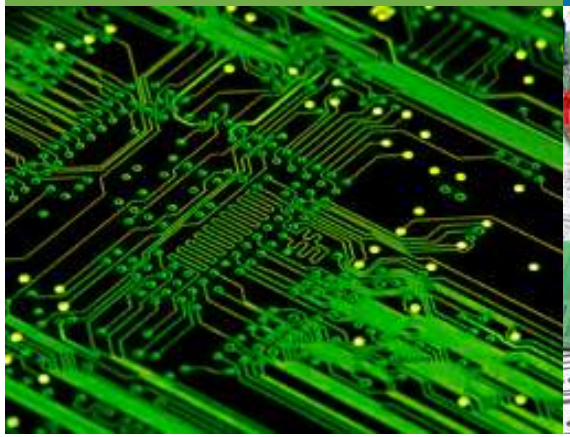
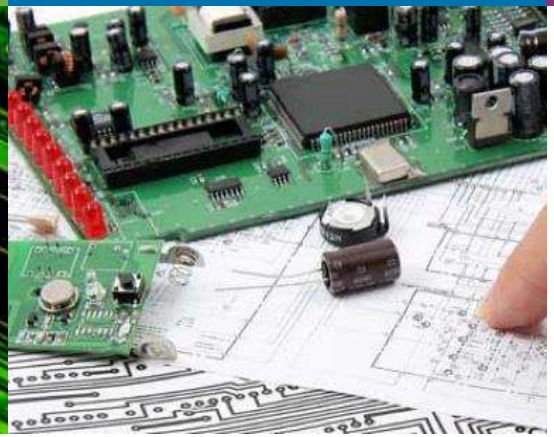
- Provide architecting and implementation services, including highly sensitive military projects
- Interface between systems engineering and internal IT services
- Unique expertise combining military systems architecture and deep understanding of electronic equipment – especially related to transportation equipment - ISO 21434 Trained and Certified personnel

- Design and build custom operational solutions using enterprise-grade technologies
- Evaluation of software and hardware system security to identify weaknesses
- Identification of cyberattack risk areas through internal audits and impact analyses on operations
- Assistance in defining and adjusting internal policies and systems to increase compliance and protection against cyberattacks
- Offering services of the CISO As A Service type

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# Related Services

## Many additional services inherent to our activities

| PCB Development | Prototype assembly end manufacturing assistance | Test Benches |
| --- | --- | --- |
|  |  |  |

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# Internal R&D / AI assisted

- Cysca strives to **continuously improve** its expertise and knowhow by initiating R&D projects and exploring new technologies.

- The EV Onboard Charger is one R&D project Cysca has initiated.

- Our goal is to learn about EV on-board battery charger technology.

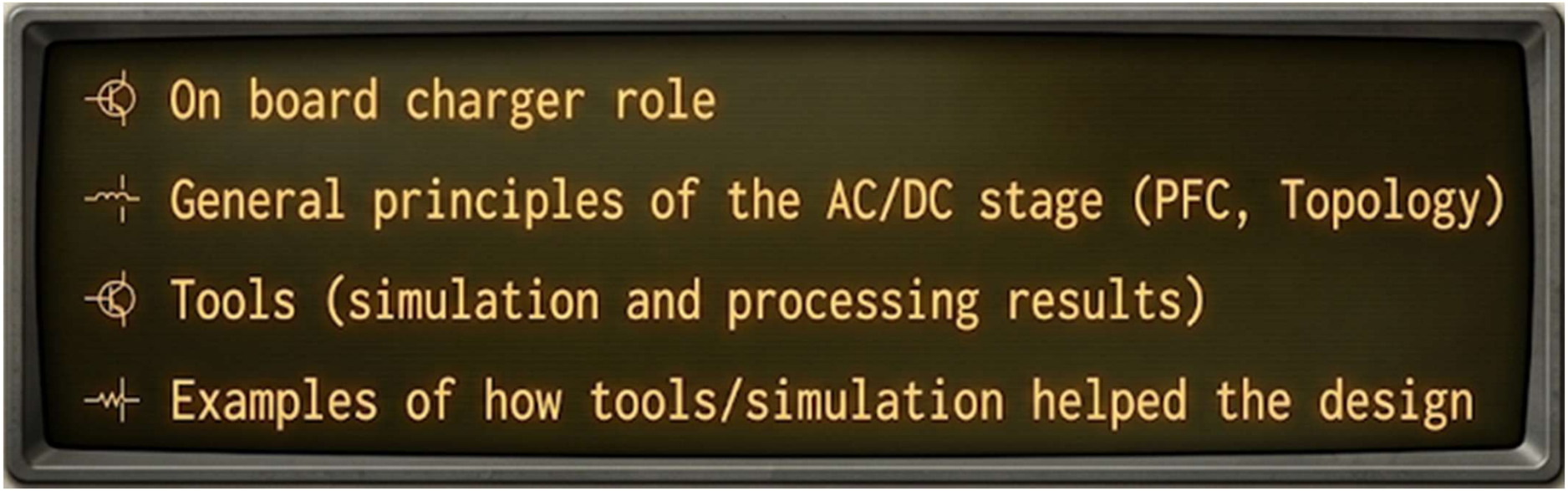
The following slides covered by Sébastien Lagacé will focus on the design of the PFC stage of the EV Onboard Charger.

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# Presentation of the R&D project

**Design and Simulation of a SiC Totem-Pole PFC for EV Onboard Charging**

**In the next slides**

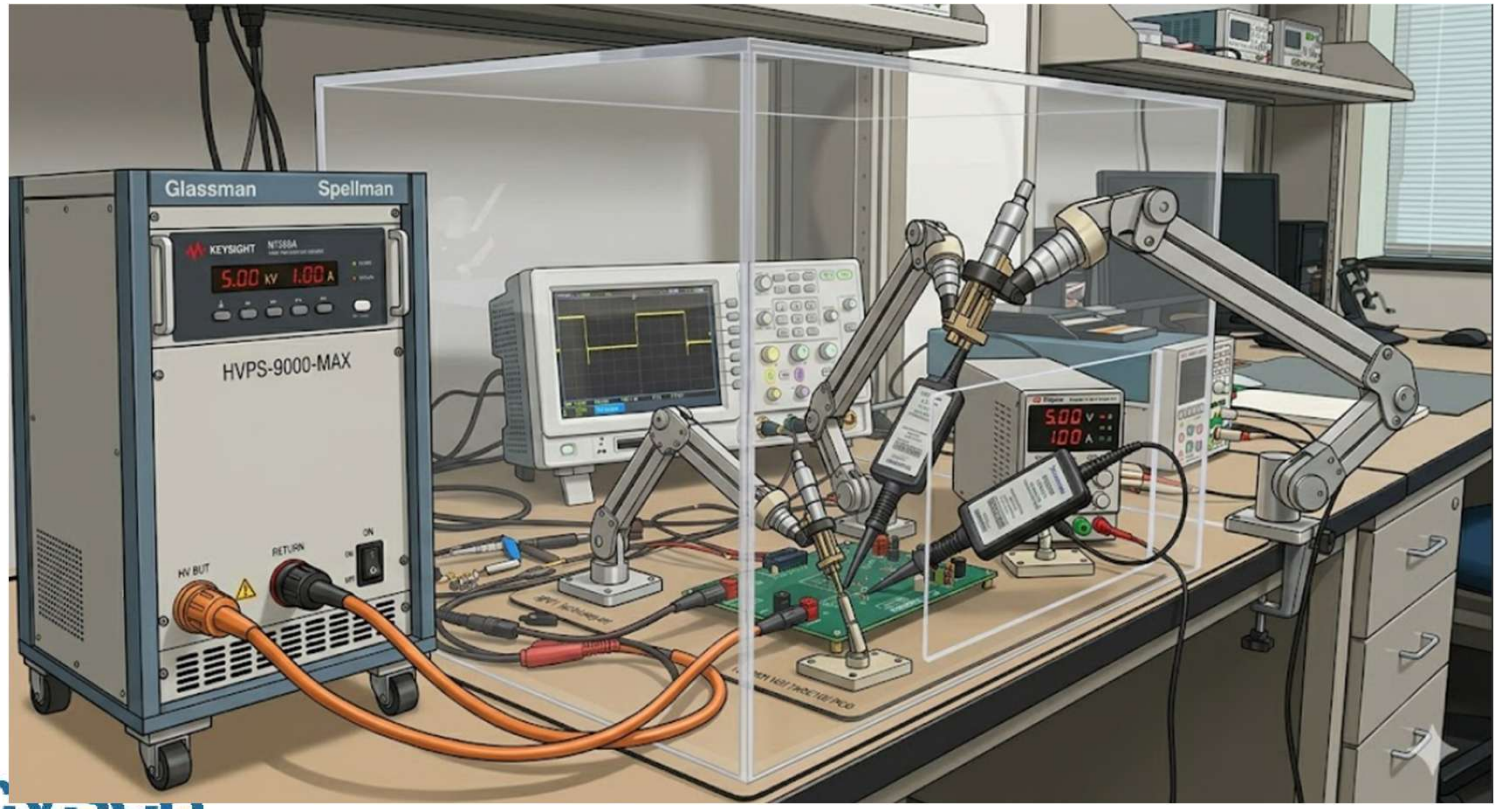



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# Realistic simulation

**Gains of realistic simulation:**

- Easily probe and debug (HV probing setup can be complex)
- Assess impact of a modification quickly
- Component sizing and design from simulation data
- Find costly design issue before it’s too late



# AI Assisted Workflow

AI was used while working on this project:

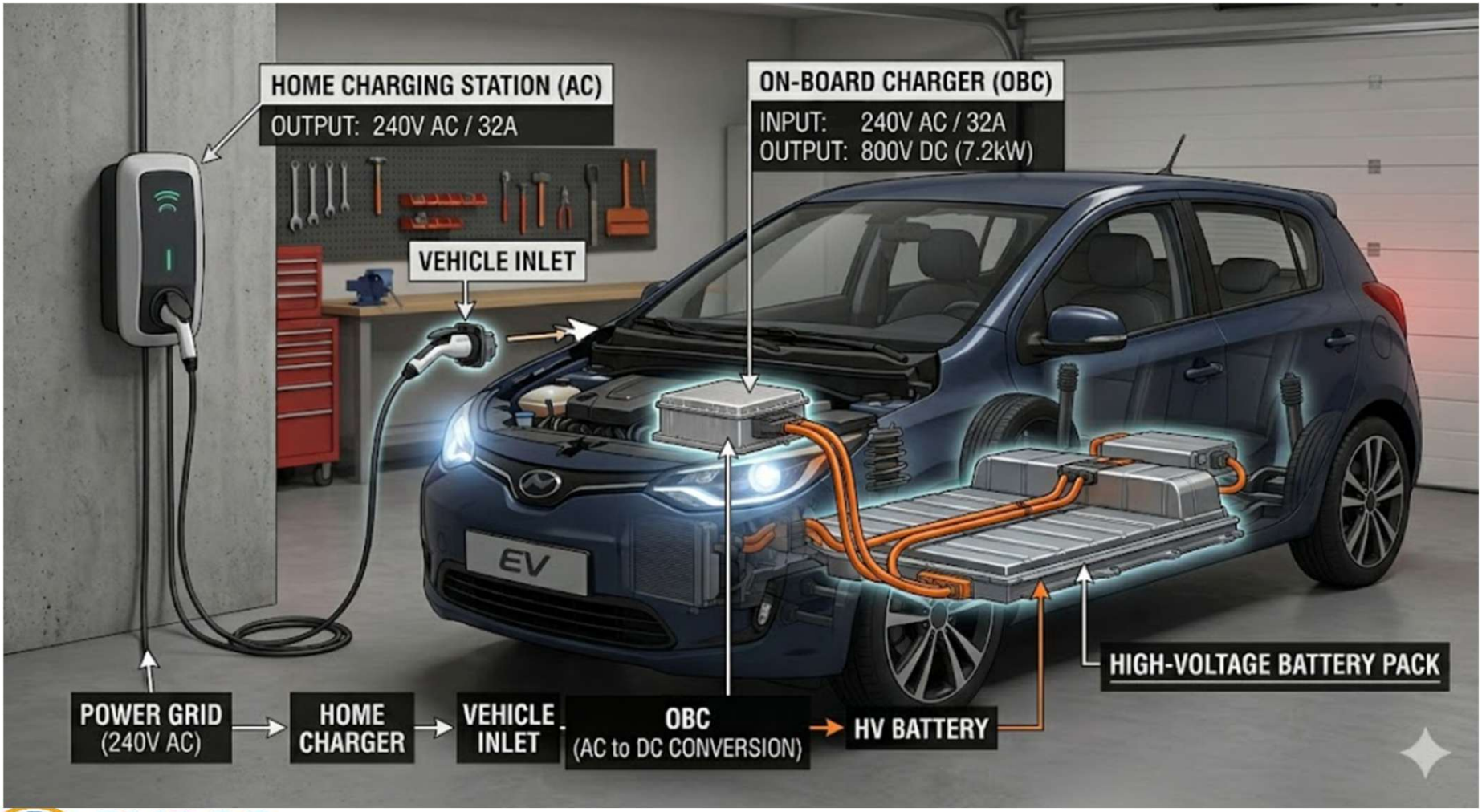
Major contributions:

- Control C++ code for simulation
- Python scripts (Calculations, post-processing of simulation data)
- Help with design (Calculation, design review/continuous improvement)

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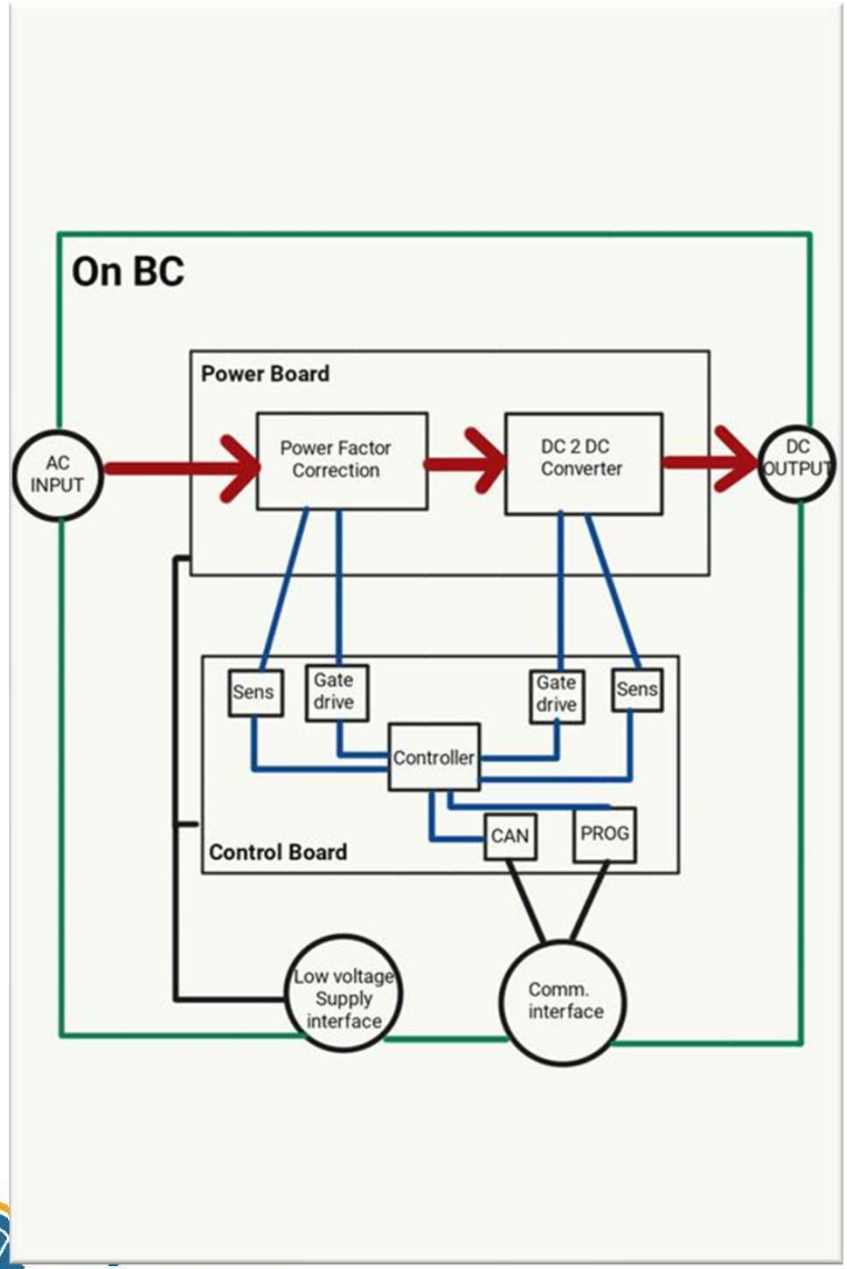
# Project Overview

The on-board charger




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# The Architecture




- AC Input: **1-phase** or 3-phases
- PFC front-end to sink almost resistive current, pure sinewave and producing 480VDC.
- DC/DC converter powered by the 480VDC and producing voltage/current for charging the battery.
- Control circuit and software.

# Project status

## Work in progress

- Simulations (very good but still some control improvements were postponed)
- Design/ schematic (in progress)

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# AC/DC power stage role

1. AC to DC conversion (480V for DC/DC stage)
2. PFC (Power factor correction)

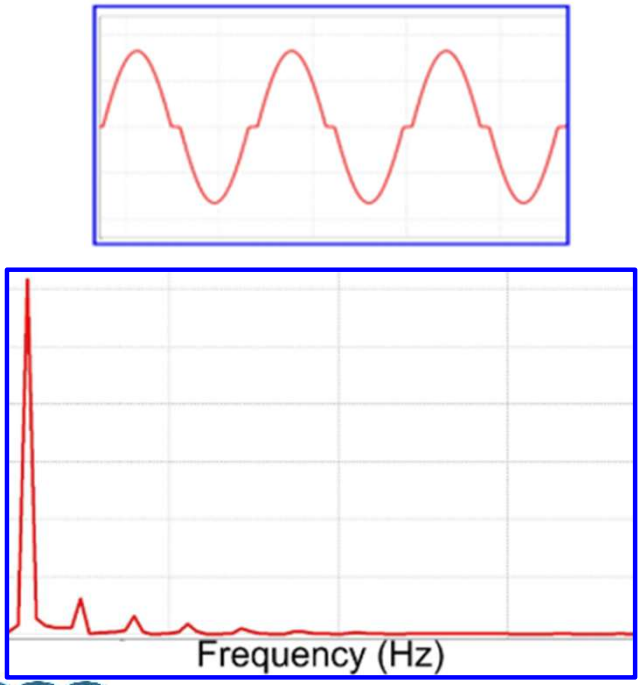


Voltage

Current

**PF close to 1 for max efficiency**

3. THD (Total Harmonic Distortion)

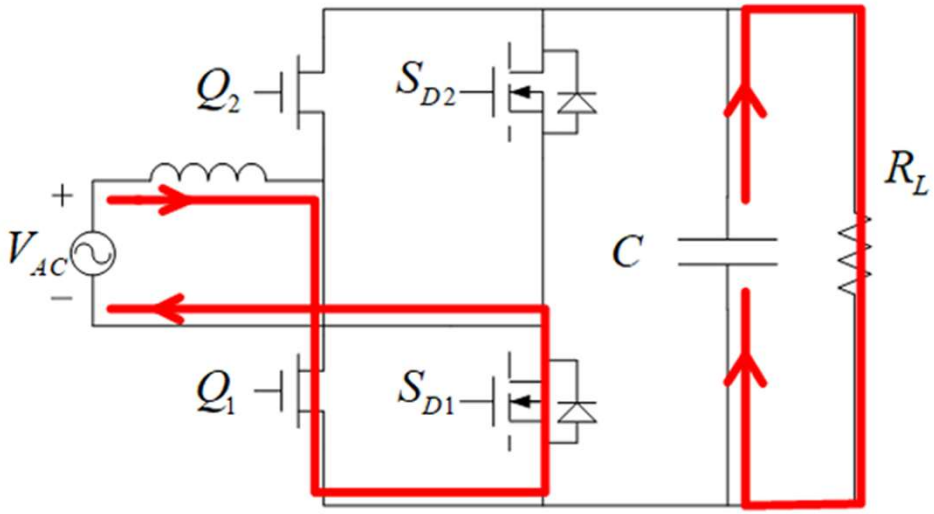



**Low THD to pass standards**

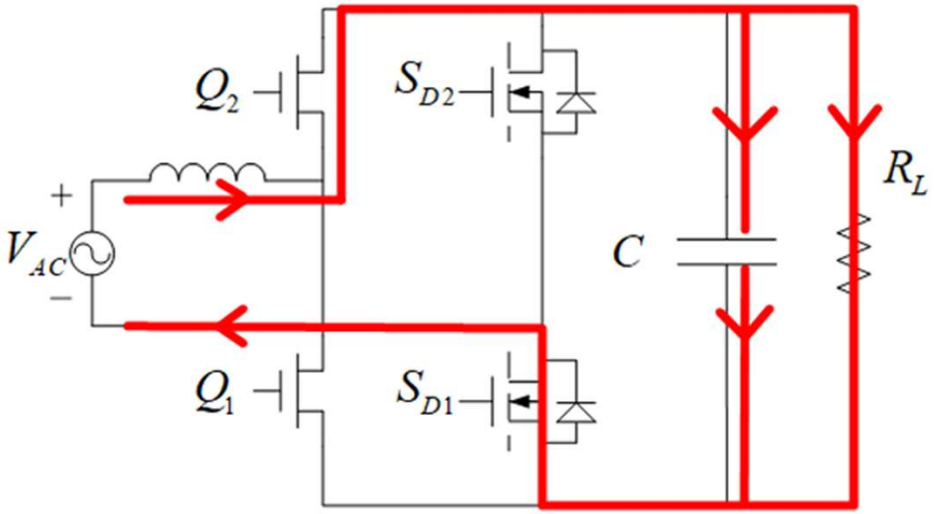
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# Totem pole operation

**Positive alternance**




a. Positive cycle charging mode




b. Positive cycle after-flow mode

**Negative alternance**

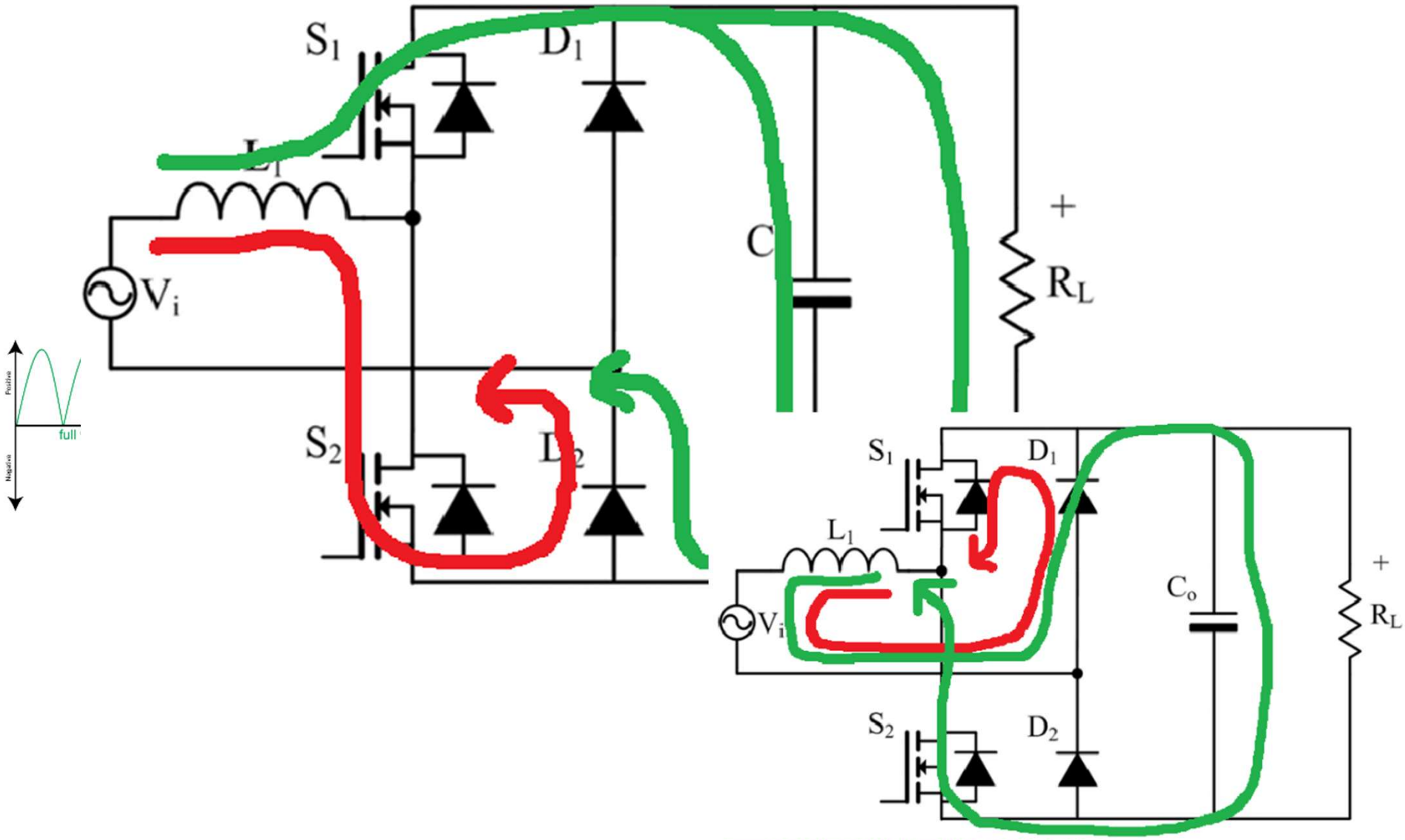
Same behavior with:
Q1 and Q2 role reversed
SD2 conduction
Inductor current reversed.

**Duty cycle**

0V-10V : Switching is stopped to manage zero crossing
50V : High duty (90%)
340V : Low duty (29%)

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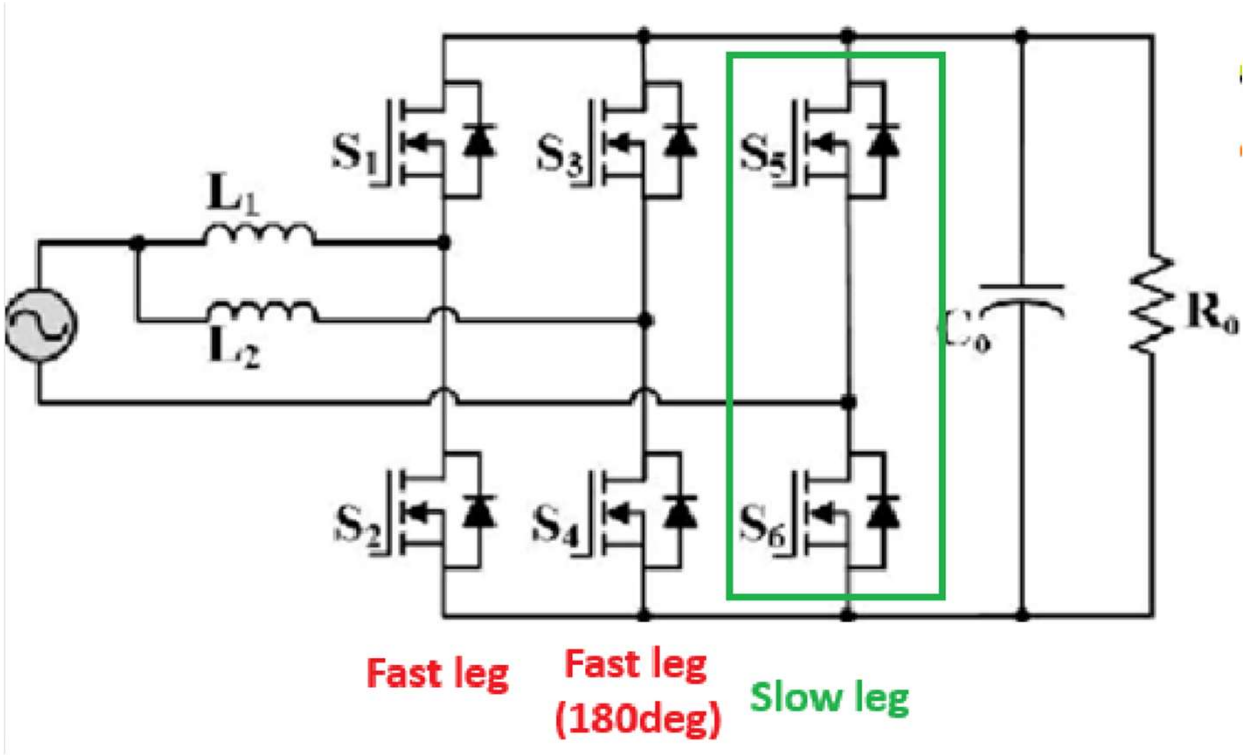
# Totem pole operation




50V : High duty (90%)
340V : Low duty (29%)

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# Interleaved + bridgeless operation




**Interleaved**

- Current per leg: /2
- Conduction losses per switch: /4
- Allows the use of smaller SM FET and simple cooling
- Ripple cancellation between legs
- Ripple frequency (260kHz to 520kHz)

**Bridgeless**

- Reduces losses compared to diodes to allow operation at 98%+ efficiency

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# Fet selection

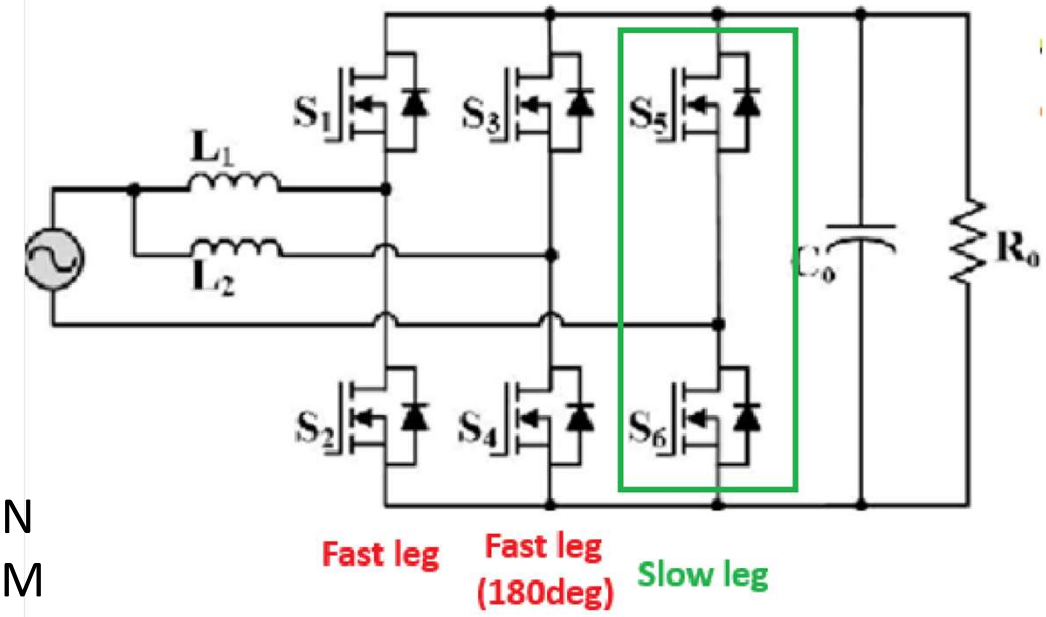
**Two different FET** :

Fast legs : half the current but fast switching

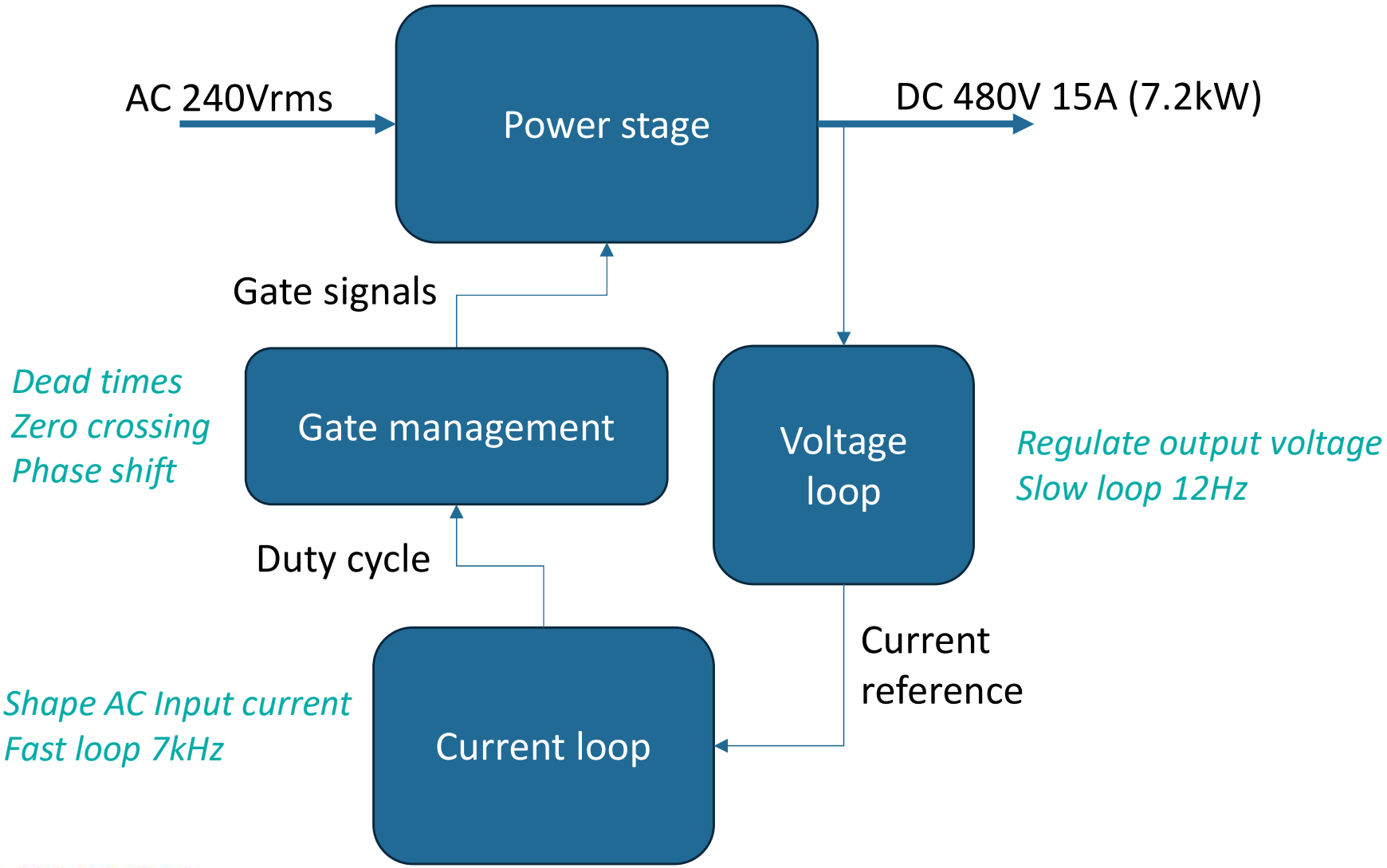
Slow leg : full current but negligible switching losses

**Why SiC FET?**

- Low switching losses
- High voltage tolerant
- Easier to cool and control than GaN
- SiC or Gan Fet are essential for CCM operation



# Control solution




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# Simulation

**Simulation tool : Qspice**



- Free
- Fast
- Easy integration of C++ code blocks

**Post processing  and Calculations : Pyhton scripts**

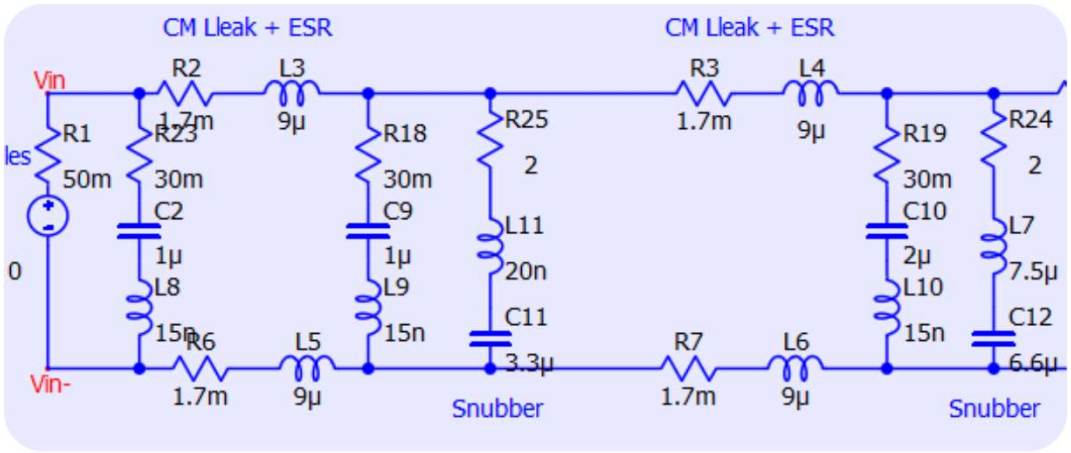


- Use Raw sim data from Qspice and analyze it
- Python = best time to result ratio

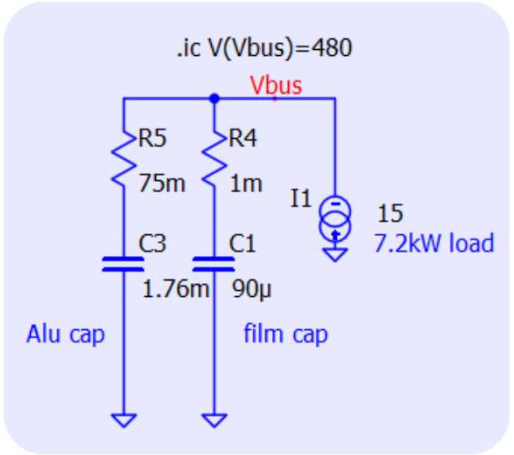
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# Simulation detail

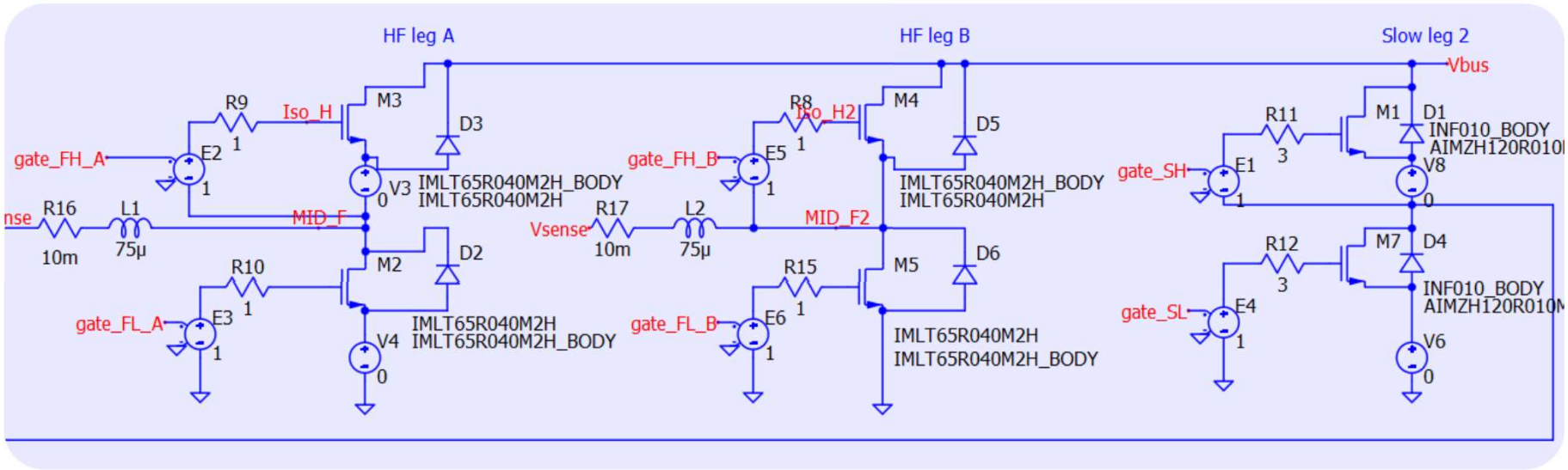
## EMI Filter and source




## Capacitor and load

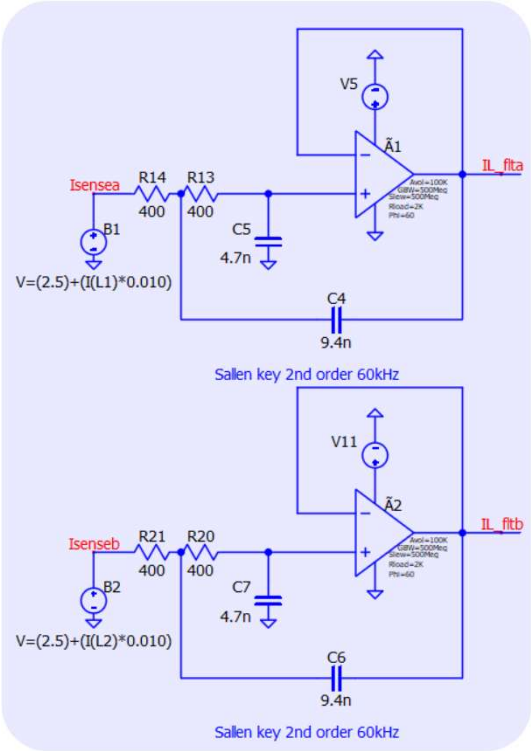



## Power stage (Fast leg x2 and Rectifier leg x1)

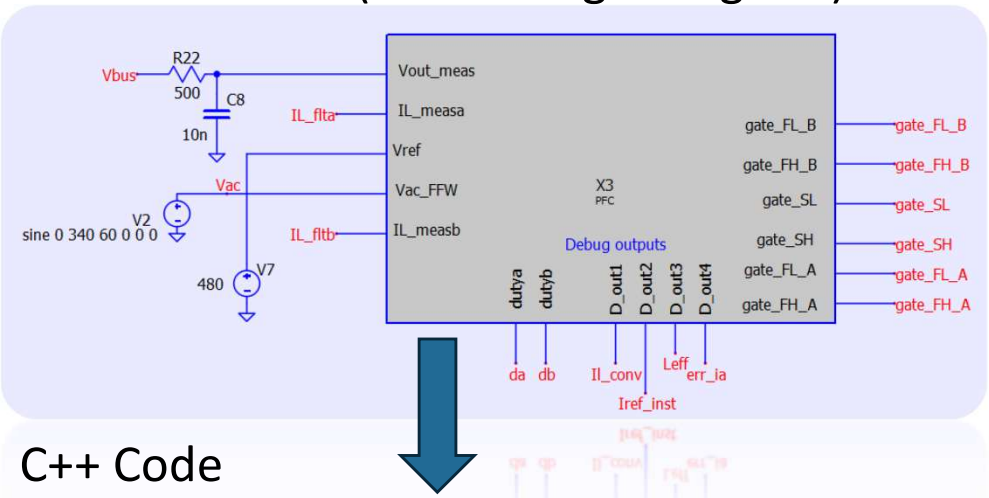


# Simulation detail

## Current sensors and filters




## Control Block (Generate gate signals)




## C++ Code

Qorvo QSPICE® - pfc.cpp

File Edit View Help

```
// ------------------------------------------------------------------------
// current_loop()
// ------------------------------------------------------------------------
static double current_loop(double IL_raw, double Vac_FFW, double Vout_meas,
                           double Iref, double Vin_peak_dyn,
                           double &u, double &e, int &soft_oc)
{
   double IL_A      = (IL_raw - 2.5) / 0.01;
   double IL_signed = (Vac_FFW >= 0.0) ? IL_A : -IL_A;
   double IL_abs    = IL_signed < 0.0 ? -IL_signed : IL_signed;

   if (!soft_oc && IL_abs >= I_SOFT_OC_TRIP)  soft_oc = 1;
   if ( soft_oc && IL_abs <  I_SOFT_OC_CLEAR) soft_oc = 0;
   double d_min = soft_oc ? 0.0 : DUTY_MIN;

   double vac_abs   = Vac_FFW < 0.0 ? -Vac_FFW : Vac_FFW;
   double Iref_inst = iref_shape(Iref, vac_abs, Vin_peak_dyn);

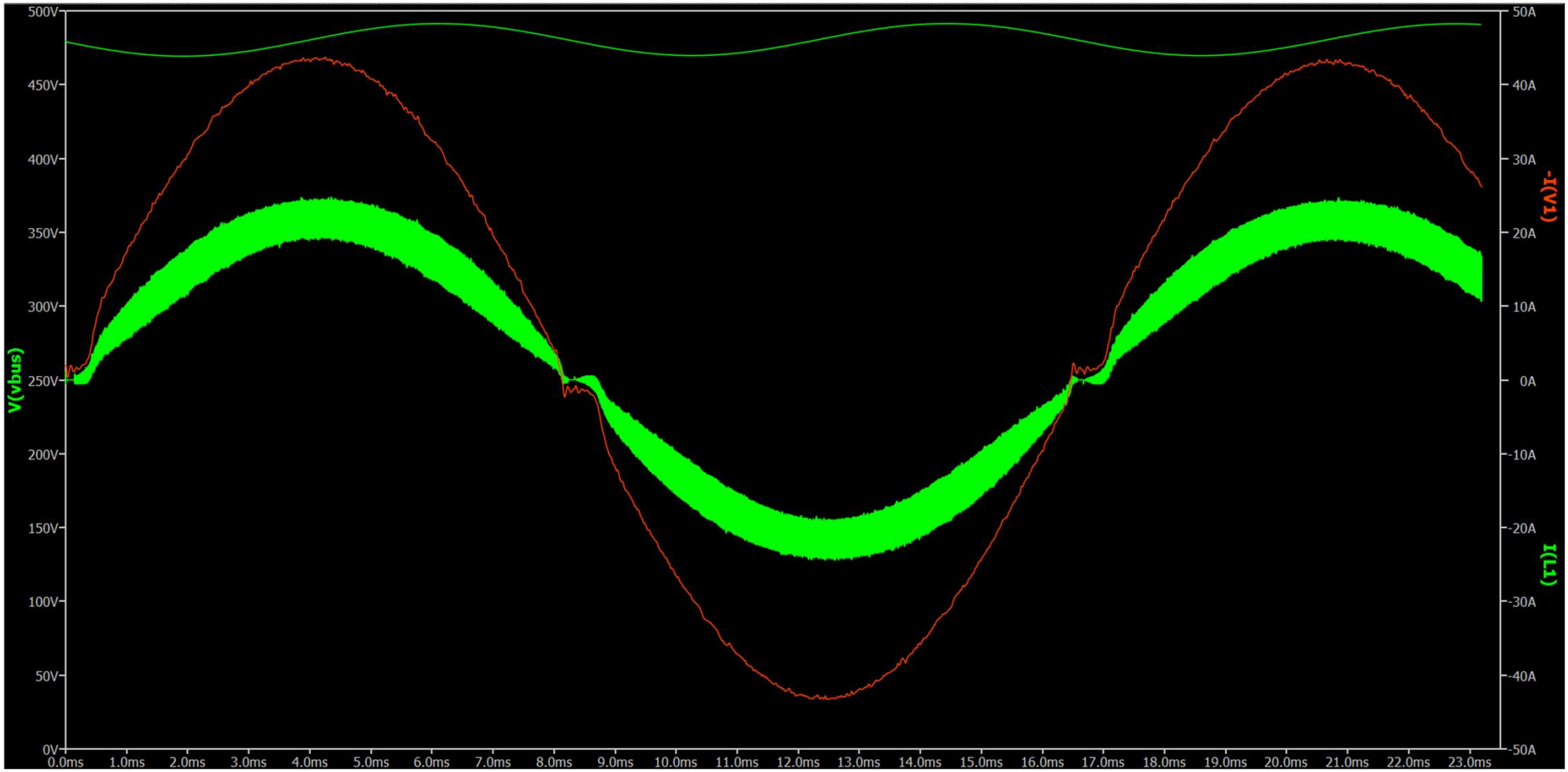
   double Vout_safe = Vout_meas > 1.0 ? Vout_meas : 480.0;
   double d_ff      = 1.0 - vac_abs / Vout_safe;
   double err_i     = Iref_inst - IL_signed;
   double d_raw     = u + b0_i * err_i + b1_i * e + d_ff;

   double d_out = d_raw < d_min ? d_min : d_raw;
   if (d_out > DUTY_MAX) d_out = DUTY_MAX;

   bool saturated = (d_out != d_raw);
```

# Simulation detail

Results from nominal simulation

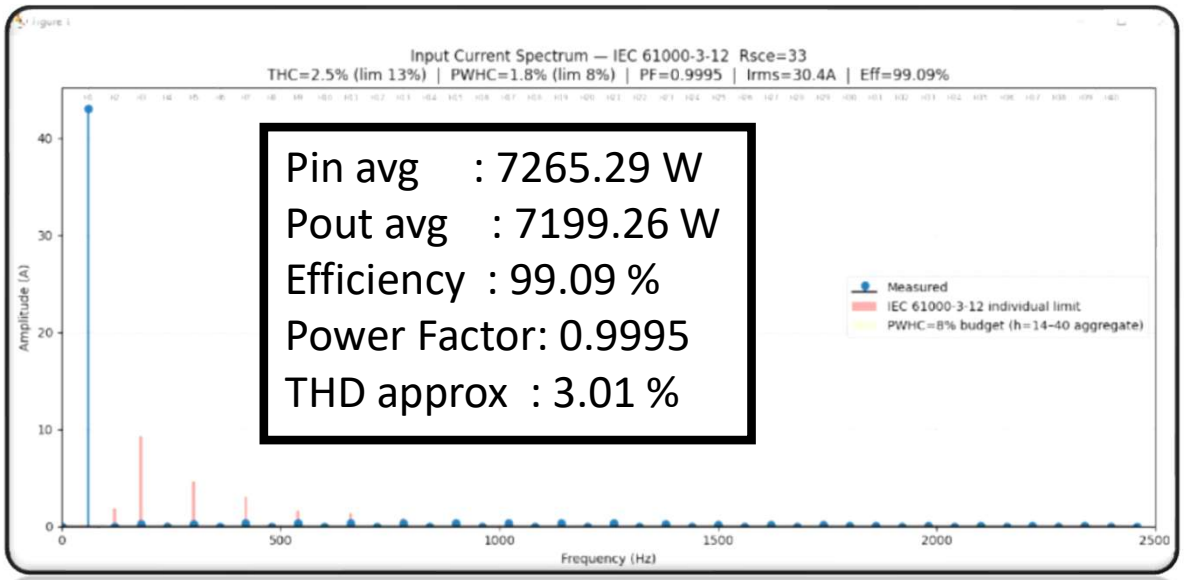



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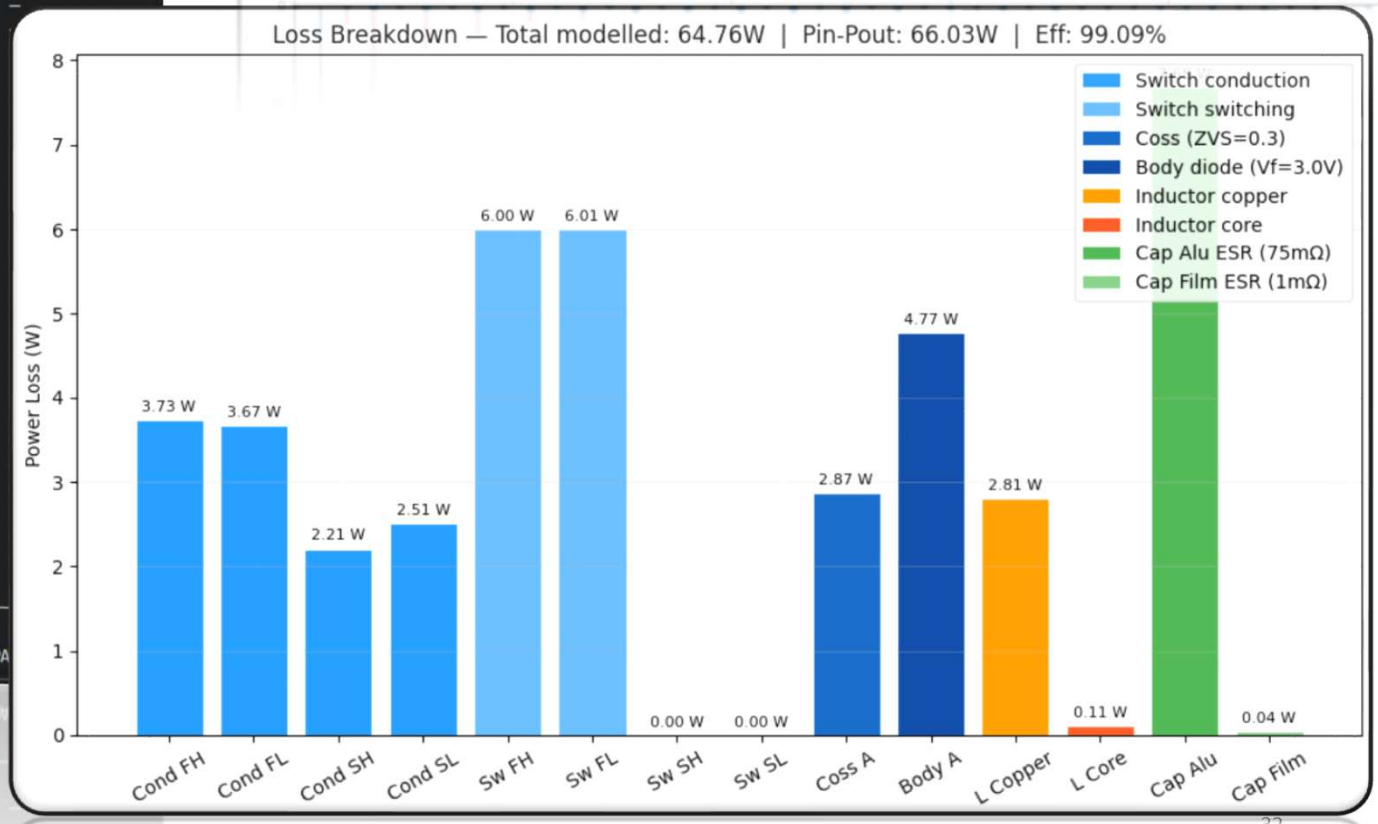
# Post processing tool

| H | Freq | Ih (A) | % of I1 | Limit % | Margin % | Status |
|---|---|---|---|---|---|---|
| 1 | 60Hz | 43.043A | 100.00% | – | – | fundamental |
| 2 | 120Hz | 0.001A | 0.00% | 4.3% | +4.30% | PASS ✓ |
| 3 | 180Hz | 0.270A | 0.63% | 21.6% | +20.97% | PASS ✓ |
| 4 | 240Hz | 0.001A | 0.00% | 1.1% | +1.10% | PASS ✓ |
| 5 | 300Hz | 0.277A | 0.64% | 10.7% | +10.06% | PASS ✓ |
| 6 | 360Hz | 0.006A | 0.01% | 0.6% | +0.59% | PASS ✓ |
| 7 | 420Hz | 0.301A | 0.70% | 7.2% | +6.50% | PASS ✓ |
| 8 | 480Hz | 0.007A | 0.02% | 0.4% | +0.38% | PASS ✓ |
| 9 | 540Hz | 0.319A | 0.74% | 3.8% | +3.06% | PASS ✓ |
| 10 | 600Hz | 0.003A | 0.01% | 0.3% | +0.29% | PASS ✓ |
| 11 | 660Hz | 0.338A | 0.79% | 3.1% | +2.31% | PASS ✓ |
| 12 | 720Hz | 0.006A | 0.01% | 0.2% | +0.19% | PASS ✓ |
| 13 | 780Hz | 0.339A | 0.79% | 2.0% | +1.21% | PASS ✓ |
| 14 | 840Hz | 0.004A | 0.01% | (PWHC) | – | |
| 15 | 900Hz | 0.347A | 0.81% | (PWHC) | – | |
| 16 | 960Hz | 0.014A | 0.03% | (PWHC) | – | |
| 17 | 1020Hz | 0.329A | 0.76% | (PWHC) | – | |
| 18 | 1080Hz | 0.009A | 0.02% | (PWHC) | | |
| 19 | 1140Hz | 0.314A | 0.73% | (PWHC) | | |
| 20 | 1200Hz | 0.014A | 0.03% | (PWHC) | | |
| 21 | 1260Hz | 0.303A | 0.70% | (PWHC) | | |
| 22 | 1320Hz | 0.007A | 0.02% | (PWHC) | | |
| 23 | 1380Hz | 0.240A | 0.56% | (PWHC) | | |
| 24 | 1440Hz | 0.006A | 0.01% | (PWHC) | | |
| 25 | 1500Hz | 0.205A | 0.48% | (PWHC) | | |
| 26 | 1560Hz | 0.002A | 0.01% | (PWHC) | | |
| 27 | 1620Hz | 0.162A | 0.38% | (PWHC) | | |
| 28 | 1680Hz | 0.018A | 0.04% | (PWHC) | | |
| 29 | 1740Hz | 0.138A | 0.32% | (PWHC) | | |
| 30 | 1800Hz | 0.024A | 0.06% | (PWHC) | | |
| 31 | 1860Hz | 0.085A | 0.20% | (PWHC) | | |
| 32 | 1920Hz | 0.013A | 0.03% | (PWHC) | | |
| 33 | 1980Hz | 0.051A | 0.12% | (PWHC) | | |
| 34 | 2040Hz | 0.002A | 0.01% | (PWHC) | | |
| 35 | 2100Hz | 0.035A | 0.08% | (PWHC) | | |
| 36 | 2160Hz | 0.018A | 0.04% | (PWHC) | | |
| 37 | 2220Hz | 0.037A | 0.09% | (PWHC) | | |
| 38 | 2280Hz | 0.015A | 0.03% | (PWHC) | | |
| 39 | 2340Hz | 0.039A | 0.09% | (PWHC) | | |
| 40 | 2400Hz | 0.007A | 0.02% | (PWHC) | | |

THC (h=2..40) : 2.49% limit 13.0% margin +10.51%
PWHC (h=14..40) : 1.77% limit 8.0% margin +6.23% PA




Pin avg : 7265.29 W
Pout avg : 7199.26 W
Efficiency : 99.09 %
Power Factor: 0.9995
THD approx : 3.01 %




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# Examples of challenges with 260kHz

## Parasitics have a larger impact at 260kHz (with fast 50V/ns ramps) :

**Parasitic capacitance from overlap**: Switch node trace to other trace:
(Overlap area : 5x5mm, Distance between layers : 32mils)

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d}$$ **1.25pF** $$I = C \cdot \frac{dV}{dt}$$ **62.5mA will circulate through the pad looking for a return path**

**Other examples**

- **Power Loop Inductance**
  - L*di/dt interaction = Severe voltage ringing.
- **Snubber Networks**
  - Requires low capacitance to prevent rapid overheating.
- **Many more.**

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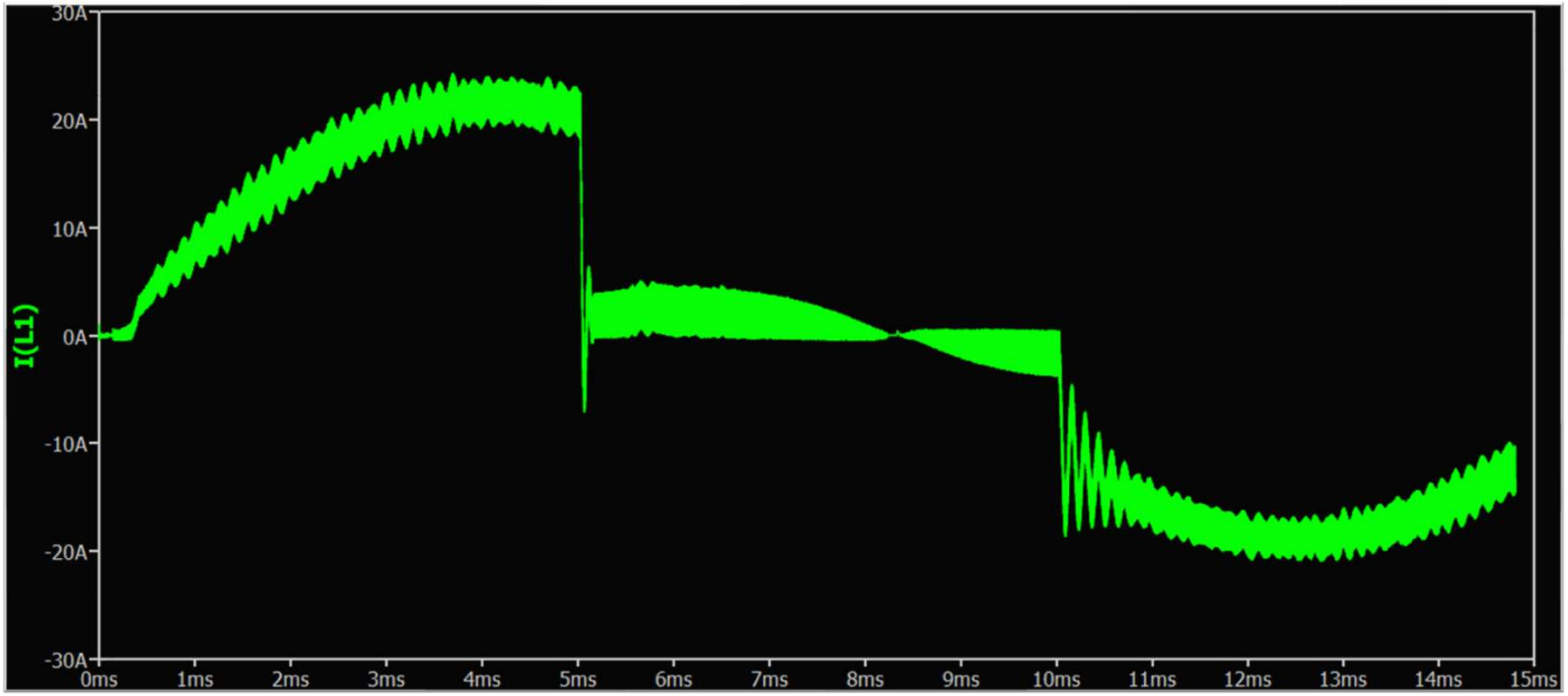
# Few examples of simulation, scripts or AI help

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# Phase margin validation through simulation

Add delay in MCU reaction until unstable (6 sw cycles = 58deg at BW)

Step on current reference reaction



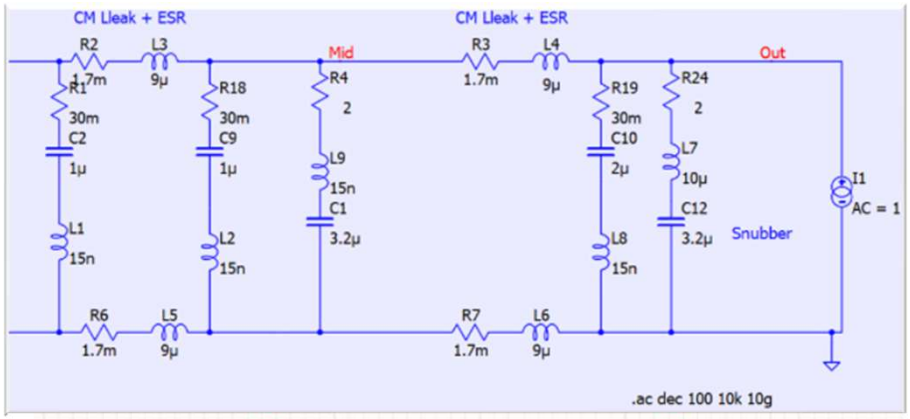

**Barely stable : Margin is close to 58deg**

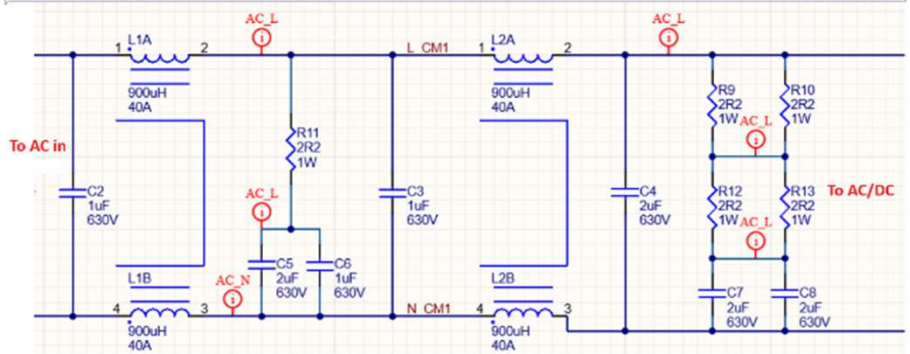
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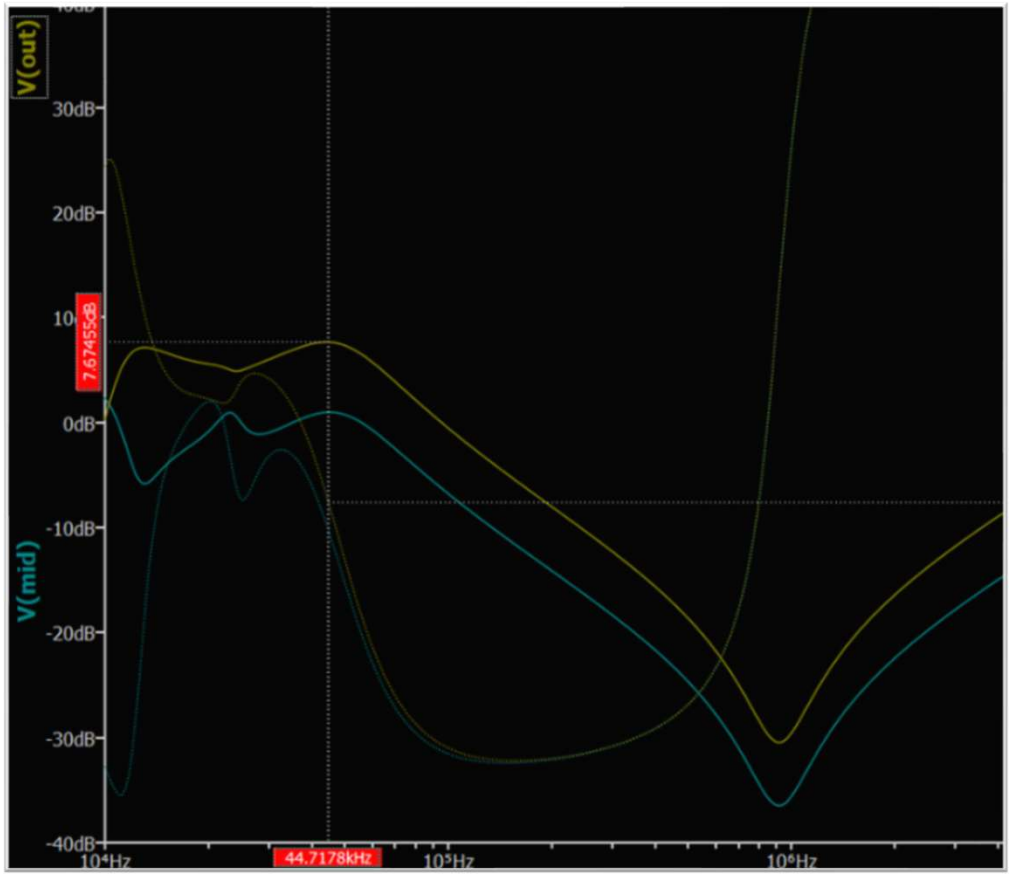
# Design EMI filter

Lleak 1-3% of common mode value can have large impact on PFC tuning and stability
Parasitic inductance variation was included in simulations

Damping the filter resonance



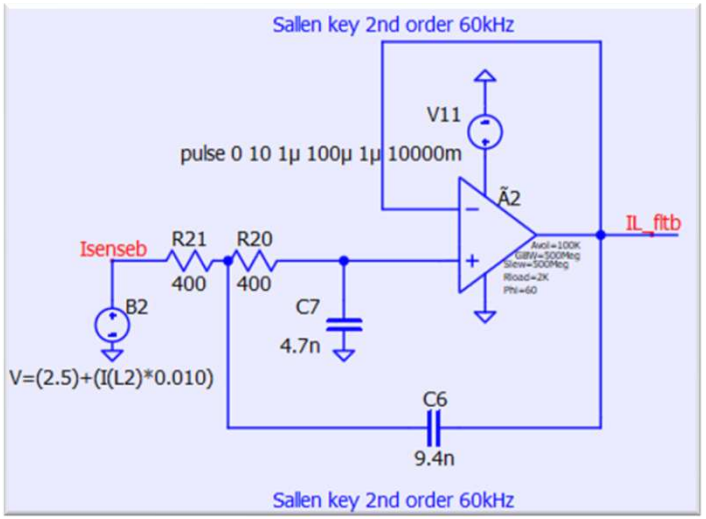

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# Current measurement

Hall effect sensor (one per interleaved legs)

## Simulation

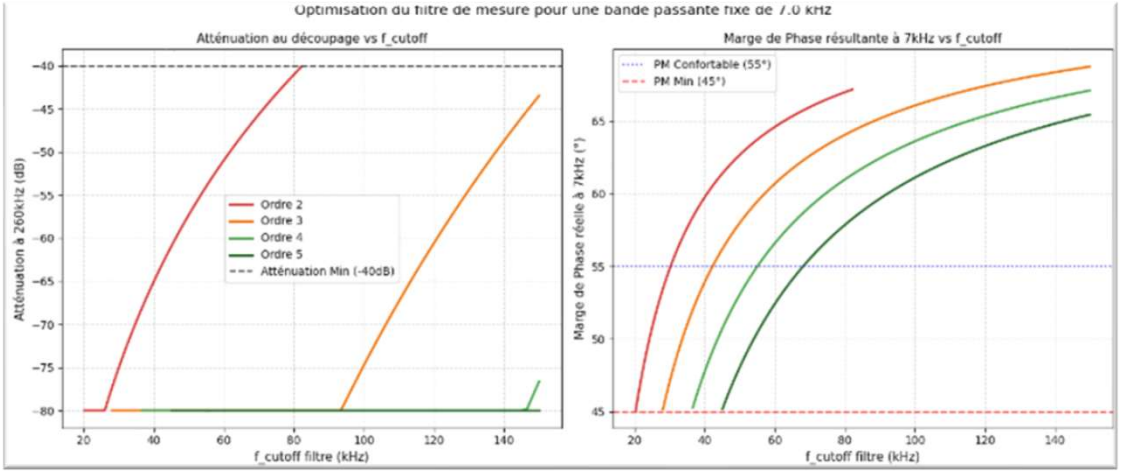
Current measurement filter




## AI script

AI generated script for optimisation of :

- Attenuation at 260kHz
- Low delay at BW frequency

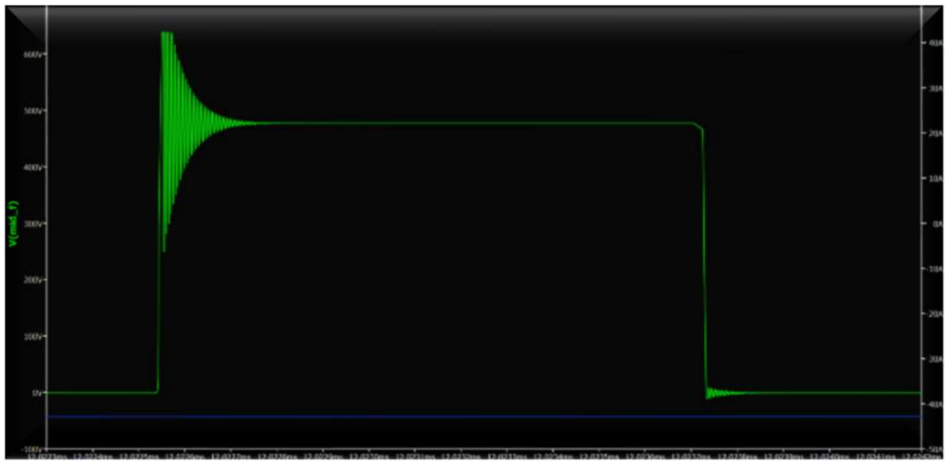


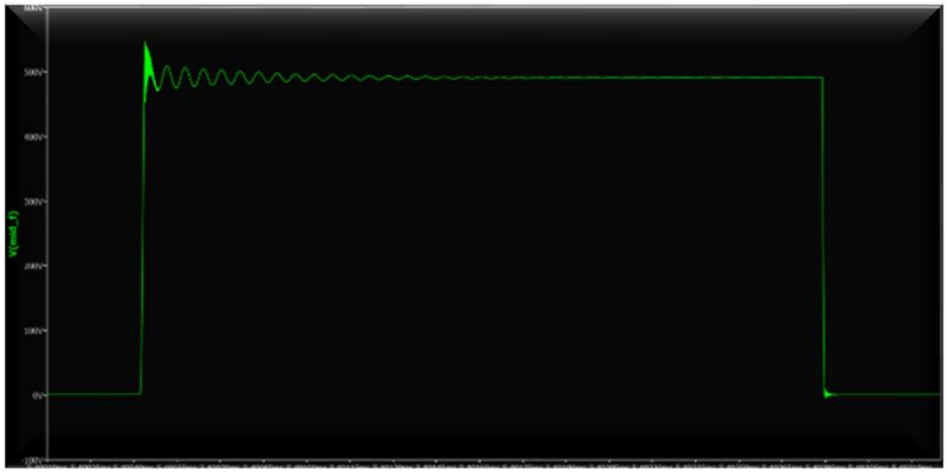

Lots of possibilities

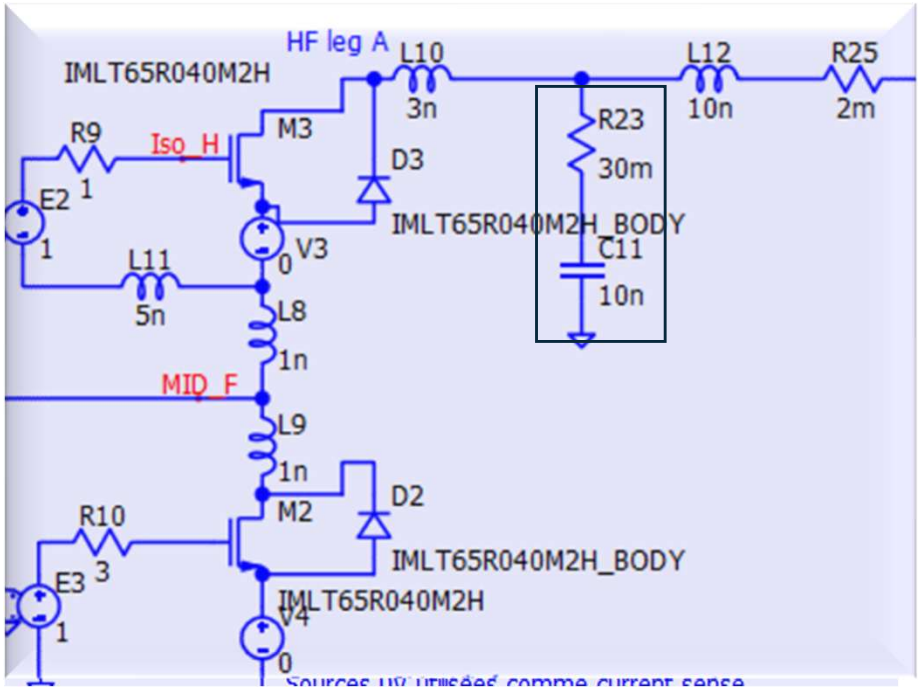
Quick comprehension of trade-offs

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# Design snubber requirement





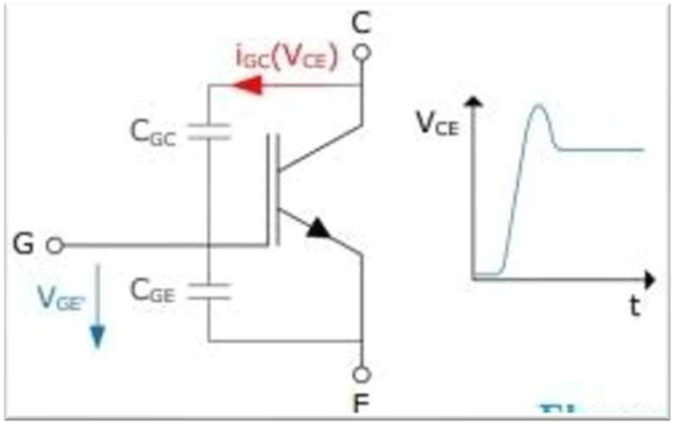


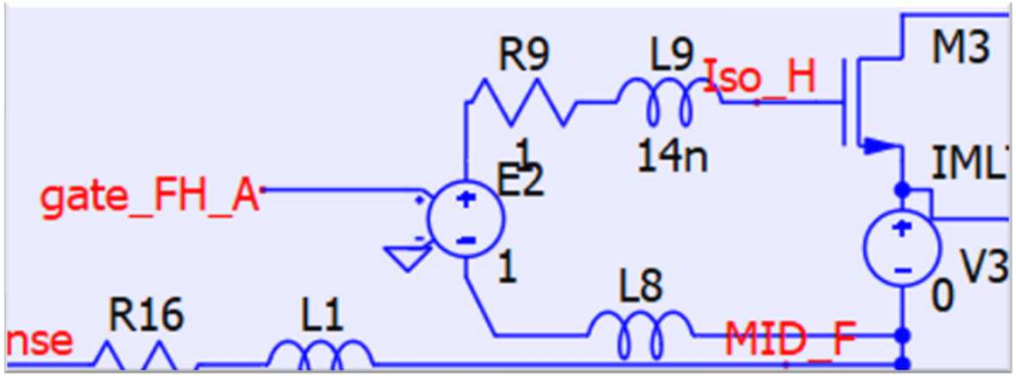

**Very good layout and well-placed high frequency cap could potentially allow no or small snubber**

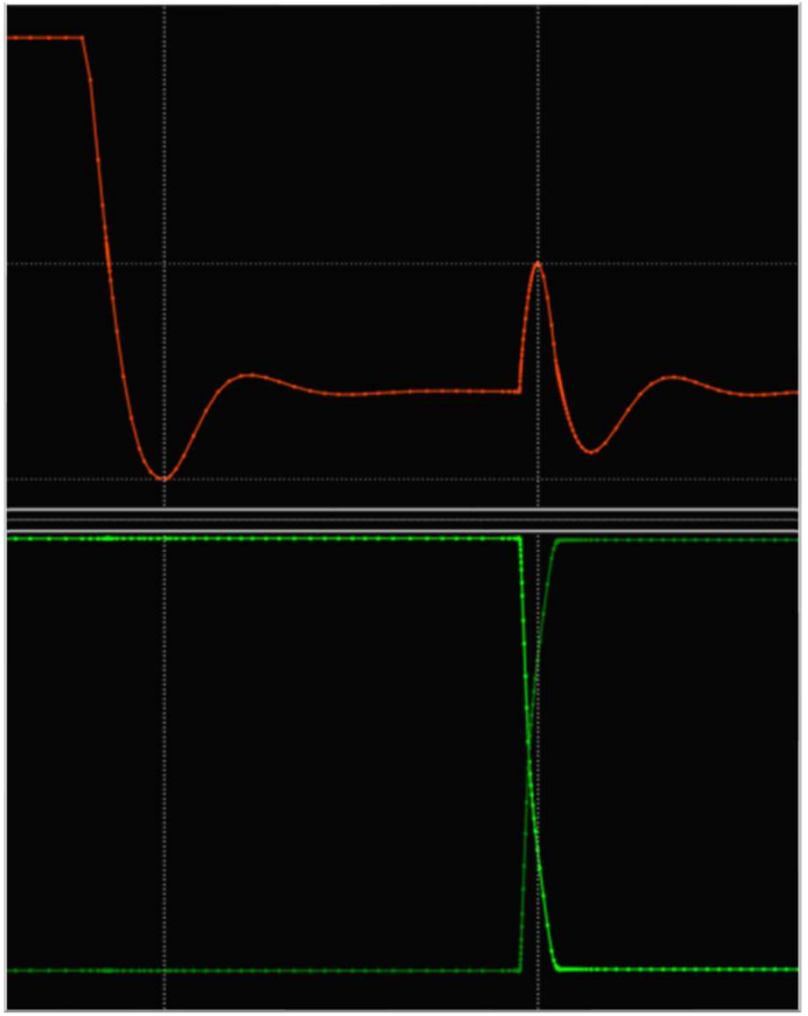
**Space for a small snubber is still planned in case.**

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# Gate driver (Miller current)



# Thank You!

Visit our kiosk or contact Cysca Technologies for your custom engineering and technology needs.

Any Questions?